British Innovators in Computing

British Innovators in Computing:

 $Early\ Industry\ Leaders$

Ву

Stephen H. Kaisler

Cambridge Scholars Publishing



British Innovators in Computing: Early Industry Leaders

Series: Historical Computing Machine Series

By Stephen H. Kaisler

This book first published 2025

Cambridge Scholars Publishing

Lady Stephenson Library, Newcastle upon Tyne, NE6 2PA, UK

British Library Cataloguing in Publication Data A catalogue record for this book is available from the British Library

Copyright © 2025 by Stephen H. Kaisler

All rights for this book reserved. No part of this book may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the copyright owner.

ISBN: 978-1-0364-5133-2

ISBN (Ebook): 978-1-0364-5134-9

TABLE OF CONTENTS

List of Figures	xiii
List of Tables	xvi
Acknowledgements	xix
Introduction	1
Industry Development	
Chapter One	4
Marconi Elliott Computer Systems	
1.1 Marconi – The Early Years	4
1.1.1 Marconi TAC	
1.1.2 The IMP	
1.2 The Myriad Family	
1.2.1 Myriad I	
1.2.2 Myriad II	
1.2.3 Myriad III	
1.2.4 I/O Systems	
1.2.5 Peripheral Devices	
1.2.6 Myriad System Software	
1.2.7 Marconi Assessment	
Chapter Two	20
GEC Computers and Automation Ltd	
2.1 GEC 2050	21
2.2 System Architecture	21
2.2.1 Arithmetic Unit	22
2.2.2 Microprogram Control	23
2.2.3 Memory	24
2.2.4 Data Transfer Methods	24
2.3 GEC 2050 Software and Support	24
2.3.1 Minisystem	24
2.3.2 Symbolic Assembler	25
2.3.3 Linking Loader	25

	2.3.4 Program Editor	26
	2.3.5 Program Checkout	26
	2.3.6 Remote Job Entry	26
	2.3.7 GEC 2050 Support	26
2.4	4 GEC 2050 Assessment	27
2.:	5 GEC 4080	27
	2.5.1 GEC 4080 System Architecture	29
	2.5.2 GEC 4080 Central Processor	32
	2.5.3 Main Memory	34
	2.5.4 I/O System	37
	2.5.5 Channel Operations	
	2.5.6 Interfaces	44
	2.5.7 Peripheral Devices	45
	2.5.8 Multiprocessor Support	46
	2.5.9 Real time Support	48
	2.5.10 GEC 4080 as a Front-End Processor	53
2.0	6 GEC 4080 Instruction Set	
	2.6.1 Operands	56
	2.6.2 Instruction Formats	
	2.6.3 32-Bit Accumulator Operations	63
	2.6.4 Operations on Operand in Store	
	2.6.5 X Register Operations	
	2.6.6 Register Operations on Y and Z	
	2.6.7 Multiple Load and Store Instructions	65
	2.6.8 Indirect Branches	
	2.6.9 Branching Instructions	
	2.6.10 Literal Instructions	
	2.6.11 Literal Operations on the X Register	
	2.6.12 Literal Operations on the Y and Z Registers	
	2.6.13 Conditional Branching Instructions	68
	2.6.14 Shift Instructions	
	2.6.15 Bit Operations	
	2.6.16 String Manipulation Instructions	
	2.6.17 Miscellaneous Operations on L	
	2.6.18 RR Format Instructions	
	2.6.19 Floating-Point Operation	
	2.6.20 Floating Point Instructions in Format L	76
2.	7 NUCLEUS	76
-	2.7.1 Processes	
	2.7.2 Segments	
	2.7.3 NUCLEUS Segments	

2.7.4 Segment Instructions	86
2.7.5 Inter Chapter Branch Instructions	
2.7.6 Interprocess Coordination	
2.7.7 Inter-process Messages	
2.8 GEC 4080 Operating Systems	
2.8.1 Core Operating System	
2.8.2 Disk Operating System	
2.8.3 OS4000	
2.9 GEC 4000 Programming Languages	
2.10 Other GEC 4000 Models	
2.10.1 GEC 4090	
2.11 GEC 63	
2.11.1 System Architecture	
2.11.2 System Software	
2.11.3 Assessment	
2.12 S-Series computers	
2.12.1 S-Seven Computer	
2.12.2 S-Two Computer	
2.12.3 S-Five Computer	
2.13 GEC Assessment.	
2.13.1 NUCLEUS	
2.13.2 Architecture Limitations	
2.13.x Merger Impact	105
Chapter Three	107
Ferranti, Ltd	
3.1 Ferranti Atlas	108
3.1 Atlas System Architecture	
3.1.1 Central Processor	111
3.1.2 Program Control	
3.1.3 Storage Hierarchy	
3.1.4 Virtual Storage	
3.2 Peripherals	
3.3 Atlas Instruction Set	
3.3.1 Floating-Point Arithmetic Instructions	
3.3.2 Indexing Operations	
3.3.3 Atlas Branching Instructions	
3.3.4 Atlas Shifting Instructions	
3.3.5 Atlas Odd/Even test Instructions	
3.3.6 Atlas B-test Register Instructions	
3.4.7 Atlas Instruction Example	

3.4 Atlas Programming	124
3.4.1 The Compiler Compiler	125
3.5 The Atlas Supervisor	127
3.5.1 Structure of the Atlas Supervisor	128
3.5.2 Job Structure	
3.5.3 Programs	132
3.5.4 Process Control	133
3.5.5 Interrupt Handling	134
3.5.6 Atlas Supervisor Assessment	
3.6 Atlas 2	135
3.6.1 System architecture	
3.6.2 Atlas 2 Software	137
3.6.3The Supervisor	138
3.6.4 Peripherals	138
3.7 Atlas Assessment	139
3.7.1 Atlas I	
3.7.2 Atlas 2 Assessment	142
3.8 Sirius	
3.8.1 Sirius Configuration	
3.8.2 Sirius Instruction Set	
3.8.3 Initial Orders	
3.8.3 Sirius Programming	
3.8.3 Sirius Assessment	
3.9 Ferranti ARGUS	
3.9.1 The First Model: ARGUS 200	
3.9.2 ARGUS 200	
3.9.2 ARGUS 100	
3.9.3 ARGUS 300/350	
3.9.4 Machine Orders	
3.10 ARGUS 400/500	
3.10.1 ARGUS 500 at TNMOC	
3.12 ARGUS 700	174
3.12.1 Other Models	
3.12.2 M700 Series	
3.12.3 Users	176
3.13 ARGUS Software	176
3 14 ARGUS Assessment	177

Chapter Four	. 178
Ferranti Orion	
4.1 System Architecture	
4.1.1 Magnetic Amplifier Technology	. 181
4.1.2 The Neuron	. 182
4.1.3 Timer	. 182
4.2 Registers	. 182
4.3 Operating Modes	. 183
4.3.1 Engineering Mode	. 184
4.4 Memory	. 184
4.4.1 Reservations	. 185
4.4.2 Backing Store	. 185
4.5 I/O System	. 185
4.5.1 Lockouts	. 186
4.5.2 I/O Initiation	. 186
4.6 Orion Instruction Set	. 186
4.7 Orion 2	. 188
4.7.1 Orion2 Extracodes	. 189
4.7.2 Effect of slow Peripherals	. 192
4.7.3 Entry to Extracodes	. 192
4.8 Orion Peripherals	. 193
4.8.1 Ampex TM2 Magnetic Tape Unit	. 194
4.8.2 ICT 593 Card Reader	. 195
4.8.3 ICT 582 Card Punch	. 195
4.8.4 Magnetic Drum	. 195
4.9 ORION Software	. 196
4.9.1 The Time-sharing System	. 196
4.9.2 Interrupts	. 197
4.9.3 Built-In Programs	
4.10 Orion 1/2 Programming Languages	
4.10.1 NEBULA	. 199
4.10.2 FORTRAN	. 200
4.10.3 Extended Mercury Autocode	. 202
4.10.4 Basic Input Language	. 202
4.11 Orion Assessment	. 202
Chapter Five	. 204
Ferranti-Packard 6000	
5.1 FP-6000 System Architecture	. 205
5.2 Central Processor	
5.3 Instruction Execution	. 207

5.4 Core Store	207
5.5 I/O System	208
5.6 Peripherals	
5.6.1 Magnetic Tapes	209
5.6.2 Magnetic Drum Type 200B	
5.7 Instruction Set	
5.8 Operating System	211
5.8.1 Program Management	211
5.8.2 Multiprogramming	
5.8.3 Managing Peripherals	
5.8.4 Handling Entry To the Executive	
5.8.5 Operator Commands	
5.8 Ferranti Assessment	
Chapter Six	217
Stantec ZEBRA	
6.1 System Architecture	222
6.1.1 The K and A switches	222
6.1.2 Control Unit	
6.1.3 The Arithmetic Unit	226
6.1.4 The Main Store	229
6.1.5 Registers	231
6.2 Instruction Set	232
6.2.1 Special Instructions	
6.2.2 Typical ZEBRA Instructions	235
6.3 I/O Systems	
6.4 Programming the ZEBRA	237
6.4.1 Simple Code	
6.5 Reminisce	
6.6 Assessment of the Stantec Zebra	238
Chapter Seven	239
Metropolitan-Vickers Company	
7.1 MetroVick 950	240
7.2 AEI 1010	241
7.2.1 Control Unit	242
7.2.2 Data Scanner	
7.2.3 I/O System	
7.2.4 Unit Record Peripherals	242
7.2.5 AEI 1010 at RAF Herndon	
7.2.6 Programming Languages	

7.2.7 AEI 1010 Assessment	244
7.3 AEI 1200	244
7.4 MVEC/AEI Assessment	245
Chapter Eight	246
EMI	
8.1 The Electronic Business Machine	
8.1.1 System Architecture	
8.1.2 Central Processor	
8.1.2.1 Instruction Execution	
8.1.3 Magnetic Drum	250
8.1.3 BMC Instruction Set	
8.1.4 Peripheral Units	
8.1.5 BMC Assessment	257
8.2 EMIDEC 1100	
8.2.1 System Architecture	
8.2.2 Operator Console	260
8.2.3 Central Processor	
8.2.4 Main Storage	
8.2.5 I/O System	
8.2.6 Peripherals	
8.2.7 Instruction Set	
8.2.8 Program Structure	
8.2.9 The EMIDEC 1100 Program Tape	
8.3 EMIDEC 2400	
8.3.1 Central Data Processor	
8.3.2 Memory	277
8.3.3 I/O System	
8.3.4 Instruction Set	
8.3.5 Magnetic Tape Systems	284
8.3.6 Peripheral Systems	
8.4 EMIDEC 3400	
8.5 EMIDEC 1100 Software	
8.5.1 Synthesis Program	
8.6 EMIDEC Assessment	287
Chapter Nine	289
Assessment of English Computing	
9.1 What Happened to the British Computing Industry	
9.1.1 Lack of Adequate Resources	
9.2 Lack of Government Support	291

Table of Contents

9.3 IBM and American Vendor's Competitiveness)
Exercises for the Reader	;
Glossary	;
References	7
Index	5

LIST OF FIGURES

- 2-1. GEC 2050 System Architecture
- 2-2. GEC 4080 Minicomputer
- 2-3. GEC 4080 System
- 2-4. GEC 4080 System Configuration
- 2-5. Typical GEC 4080 System Configuration
- 2-6. GEC 4000 C Register
- 2-7. GEC 4080 CP Architecture
- 2-8. GEC 4080 Program Chapter Allocation
- 2-9. Virtual to Physical Address Mapping
- 2-10. Route Table Entry
- 2-11. WCB Format
- 2-12. Semaphore Structure
- 2-13. Process Vector Entry
- 2-14. Process Transitions
- 2-15. GEC 4080 as Front End Processor
- 2-16. GEC 4000 C Register
- 2-17. GEC 4000 A1 Format
- 2-18. GEC 4000 A2 Format.
- 2-19. GEC 40000 A3 Format
- 2-20. GEC 4000 A3 Format Addressing
- 2-21. GEC 4000 A4 Format
- 2-22. GEC A4 Format addressing
- 2-23. GEC 4000 A5 Format
- 2-24. GEC 4000 L Format
- 2-25. GEC 40000 B Format
- 2-26. GEC 4000 RR Format
- 2-27. Multiple Store Locations
- 2-28. GEC 4000 Shift Specification
- 2-29. GEC 4080 Virtual Address Mapping
- 2-30. SST Entry Contents
- 2-31. GEC 4080 Virtual to Physical Address Mapping
- 2-32. Master Segment Structure
- 2-33. CST Entry
- 2-34. GEC NUCLEUS Segment Tables
- 2-35. Route Table Entry Forma

- 2-36. Chapter Descriptor
- 2-37. NUCLEUS Message Parameters
- 2-38. CALL Instruction Format
- 2-39-SBA Buffer Format
- 3-1. The Ferranti Atlas Operator Console
- 3-2. Atlas System Architecture
- 3-3. Ferranti Atlas One-level Store Concept
- 3-4. Atlas Instruction Format
- 3-5. Central Store Address Structure
- 3-6. Sample Atlas Autocode Program
- 3-7(a) Lines for Handling EXPR
- 3-7(b). Lines for handling Assignment to Variable
- 3-7(c). Routines for Generating Compiler Code
- 3-8 Structure of the Atlas Supervisor
- 3-9. Titan Computer
- 3-10. Atlas 2 System Architecture
- 3-11. Ferranti Sirius in an Office Environment
- 3-12. Ferranti Sirius Computer
- 3-13. Sirius Operator Console
- 3-14. Sirius Rear View
- 3-15. Sirius System Architecture
- 3-16. Ferranti Sirius Delay Line
- 3-17. Ferranti Sirius Display and Console
- 3-18. Sirius Instruction Format
- 3-19(a). Victoria Ferranti Sirius CPU
- 3-19(b). Museums Victoria Ferranti Sirius Memory Unit
- 3-20. Argus Printed Circuit Cards
- 3-21. Argus Box
- 3-22. Ferranti ARGUS Console and Program Board
- 3-23. Ferranti ARGUS Computer System
- 3-24. ARGUS Order Format
- 3-25. Ferranti Argus 700 Operator Console
- 3-26. Argus 700 Computer
- 4-1. Ferranti Orion Operator's Console
- 4-2. Ferranti Orion CPU Cabinets
- 4-3. Ferranti Orion 1/2 Instruction Format
- 5-1. Magnetic Drum Type 200B
- 5-2. FP-6000 Instruction Format

- 6-1. Stantec ZEBRA System Configuration
- 6-2. ZEBRA Units Mated to Printed Circuit Board
- 6-3. Stantec ZEBRA
- 6-4. ZEBRA System Architecture
- 6-5. ZEBRA Control Unit System Architecture
- 6-6. ZEBRA Arithmetic Unit
- 6-7. ZEBRA Circuit Module
- 6-8. Modules Plugged into a Backplane
- 6-9. ZEBRA Magnetic Drum
- 6-10. Stantec ZEBRA Instruction Format
- 7-1. Metrovick 950
- 7-2. AEI 1010 at RAF Herndon
- 8-1. EMI Electronic Business Machine
- 8-2. BMC System Architecture
- 8-3. BMC Instruction Format
- 8-4. Samsatronic Printer
- 8-5. EMIDEC 1100
- 8-6. EMIDEC 1100 System Architecture
- 8-7. EMIDEC 1100 Operator Console
- 8-8. EMIDEC 11000 Operator Panel
- 8-9. EMIDEC 1100 Scope Panel
- 8-10. EMIDEC 1100 Switches
- 8-11. EMIDEC 1100 Tape Drives
- 8-12. EMIDEC 1100 Instruction Format
- 8-13. Sample Code for Computing x10
- 8-14. An EMIDEC 2400 Installation
- 8-15. EMIDEC 2400 Instruction Format
- 8-16. Simple Arithmetic Instructions

LIST OF TABLES

- 2-1. GEC2050 Basic Characteristics
- 2-2. Program Accessible Registers
- 2-3. Program Non-accessible Registers
- 2-4. Data Transfer Methods
- 2-5. GEC 4080 Basic Characteristics
- 2-6. GEC 4080 Registers
- 2-7. BMC SIGNAL Codes
- 2-8. Error Codes
- 2-9. INT Variants
- 2-10. Semaphore States
- 2-11. PV Entry Descriptions
- 2-12. PV Entry Fields Interpretation
- 2-13. Process Transitions
- 2-14. Instruction Formats
- 2-15. C Register Bit
- 2-16. Operand Notation
- 2-17. A2 Base Register Use
- 2-18. A4 Base Register Use
- 2-19. A5 Base Register U
- 2-21. Fixed-Point Operations
- 2-22. Operations on Store
- 2-23. X Register Operations
- 2-24. Y and Z Register Operations
- 2-25. Multiple Load/Store Operations
- 2-26. Indirect Branching Operations
- 2-27. Literal Instructions
- 2-28. Literal Operations on the X Register
- 2-29. Literal Operations on the Y and Z Register
- 2-30. Conditional Branching Instructions
- 2-31. Shift Operations
- 2-32. GEC 4000 Shift Types
- 2-33. Bit Manipulation Operations
- 2-34. Bit Manipulation Instructions
- 2-35. String Manipulation Instructions

- 2-36. Miscellaneous Operations on L
- 2-37. Result Size Based on Input Register Size
- 2-38. RR Format Instructions
- 2-39. Floating Point Instructions
- 2-40. Floating Point Format Instructions
- 2-41. Master Segment Description
- 2-42. Segment Manipulation Instructions
- 2-43. Inter-Chapter Branch Instructions
- 2-44. Message Sending Options
- 2-45. State Change Options
- 2-46. SBA Description
- 2-47. TYPES OF BUFFERED SYSTEMS
- 2-48. COS Programs and Capabilities
- 2-49. OS/4000 Programming Languages
- 3-1. Atlas Basic Characteristics
- 3-2. Floating Point Arithmetic Instructions
- 3-3. Atlas Indexing Operations
- 3-4. Atlas Branching Operations
- 3-5. Atlas Counting Operations
- 3-6. Atlas Shifting Operations
- 3-7. Atlas Odd-Even Test Operations
- 3-8. Atlas B-Test Register Operations
- 3-9. Atlas 2 Unit Record Equipment
- 3-10. Ferranti Sirius Basic Characteristics
- 3-11. Sirius Instruction Set Commonly Used Functions
- 3-12. Argus I/O Equipment
- 3-13. ARGUS Basic Characteristics
- 3-14. ARGUS Address Specification
- 3-15. ARGUS Address Allocation
- 3-16 ARGUS Order Codes
- 4-1. Ferranti Orion Basic Characteristics
- 4-2. ORION 1 Registers
- 4-3. Orion Instruction Fields
- 4-4. Orion 2 Extracodes
- 4-5. Extracode Data
- 4-6. Time-sharing Interruptions
- 5-1. FP-6000 Basic Characteristics
- 5-2. Instruction Execution Beats

- 5-3. Peripheral Data Transfer Beats
- 5-4. EXECUTIVE Operator Commands
- 6-1. ZEBRA Basic Characteristics
- 6-2. ZEBRA A,K Switch Combinations
- 6-3. ZEBRA Magnetic Drum Track Allocation
- 6-4. Register Usage
- 6-5. STANTEC ZEBRA Instruction Bits
- 6-6. V Bit Interpretation
- 6-7. Special Instructions
- 6-8. Typical ZEBRA Instructions
- 8-1. BMC Basic Characteristics
- 8-2. BMC Instructions
- 8-3. Interpretation of 'm' for Input
- 8-4. Interpretation of 'm' for Output
- 8-5. EMIDEC 1100 Basic Characteristics
- 8-6. Operator Panel
- 8-7. EMIDEC Register Allocation
- 8-8. Instruction Fields
- 8-9. EMIDEC 1100 Instructions
- 8-10. Dummy Instructions
- 8-11. EMIDEC 2400 Basic Characteristics
- 8-12. Condition Register Bits
- 8-13. Data Transfer Instructions
- 8-14. Literal Instructions
- 8-15. Multiplication Instructions
- 8-16. Division Instructions
- 8-17. Logical Instructions
- 8-18. Shift Instructions
- 8-19. Magnetic Tape Instructions
- 8-20. Comparison Instructions
- 8-21. Switch-Setting Instructions
- 8-22. Jump Instructions
- 8-23. Data Conversion Instructions
- 8-24. Operator Console Instructions
- 8-25. Stop Instruction

ACKNOWLEDGEMENTS

This second volume has required an extensive amount of research to find information about the English computer systems. This involved repeated searches of the Web to ferret out often hidden or differently labeled documents. Some members of the Computer Conservation society have suggested places to look and repositories of documents. I thank them very much as well as for their hospitality at CCS meetings I have attended.

The amount of documentation to read through to make sure I have done my due diligence has amounted to over 500 articles, books, reports, brochures, and manuals. This has taken considerable time, but I hope the reader will find the amount of information captured here to be helpful in understanding these systems.

I must acknowledge the family cats – Scooby Doo, Tatiania, and Boris – who have kept me company by sitting on my desk or flopping on my keyboard while I am digesting data or writing. Sadly, Scooby passed away recently after 17-1/2 years of companionship and will be greatly missed.

I dedicate this book to my wife, Chryl, for her forbearance as I spent many days and nights writing these two books.

I thank my daughter, Rebecca, a solicitor extraordinaire, who has read through this book and suggested numerous edits that have greatly increased its readability and understandability.

Introduction

INDUSTRY DEVELOPMENT

The British Computing community consisted of a diverse array of companies and universities developing machine from the early 1950s through to the 1980s. Some of these machines have been described in Birthing the Computer: From Relays to Vacuum Tubes and Birthing the Computer: From Drums to Cores. The volume English Computing Systems: Pioneering Innovation described the three major firms that designed, developed, and delivered most of these machines. This volume focuses on the contributes of some of the smaller companies and several of the major universities that also developed their own machines.

In *Pioneering Innovation*, computer development was led by several British firms which came up through the electronics industry (Elliott, English Electric) and by a tea shoppe (LEO). Each of the three manufacturers in the first volume seemed to have the financial heft to be able to undertake a research and development program in computing. The continued development of an indigenous computing industry followed a similar path by smaller companies responding to several needs of their respective industries.

As Gandy (1994) noted, the electronics companies entered the computer industry with the belief that their experience in mass producing electronics could be transferred to the rapidly developing computer marketplace in the later post-war years. Each firm tried to leverage its advantage(s) within its respective industrial domains and to enter new sectors due to its work for the military during the war to apply it to civilian demands while depending on lessening the barriers to entry.

He noted in the US, many larger firms bought smaller electronics firms for their knowledge and capabilities, while in the UK, ICT in particular bought the failing divisions of computer firms. IBM was the exception as its skills were home grown.

The British market for computing systems was not large enough to sustain multiple vendors. Eventually, the British government stepped in to force a consolidation of the different vendors into a single firm that it was 2 Introduction

hoped was both viable and profitable to carry British computing into the 1990s. This consolidation resulted in a single firm, International Computers, Ltd. (ICL), as the successor to the multiple British computer vendors.

As Gandy (1994) noted, English electronics firms failed for several reasons:

- 1. Capital Allocation: Entering the computer industry was capital intensive. Trying to maintain and enhance its existing product lines to keep up with consumer demands for new features, while developing manufacturing capabilities for computing machines was throttled by the capital demands of existing product lines. With limited capital available, hard choice favored existing product lines.
- 2. Status of the Computer division: The most push for investing in the development of new computing machines was provided by junior executives in the electronic firms. English management was a very caste conscious system in which decision-making power for the firm was wholly invested in senior management form the older divisions. They didn't understand the technology and were threatened by computers taking over some of the functions performed by their older products (now becoming obsolete.
- 3. Low Emphasis on Sales: Many electronics firms did not see the computer as product that had to be sold. In fact, they may have been a certain hubris that its rapid emergence in many areas would sell itself. Companies that saw sales as their major function (such as IBM and NCR as business machine manufacturers) were successful, while electronic firms used to selling to a limited number of agencies, utilities, and the government were not (perhaps, because their market was much smaller than the consumer market).
- 4. Financing Sales: Computers were expensive machines (including their peripherals). Customers were not used to buying such machines outright, but leasing them form the vendors. Most electronic firms were used to selling their products directly to customers with full payment in return. With leasing, the full price of the machine was not recovered for years, which meant that a different cost allocation and budgeting mechanism has to be devised.
- 5. Scale and Scope: While economies of scale did less barriers to market entry, many firms operated separate profit centers which led to barriers between divisions and competition. This led to limited, if any, sharing of resources and often locked computer divisions to buying from other divisions in the company due to vertical integration. This meant they were unable to take advantage of specialist firms developing subsystems (disk,

peripherals, electronics, etc.) developed by Texas Instruments, Motorola, Ampex, etc.

Together, these factors hobbled the agility of English computer vendors to adapt to changing market conditions. In order to maintain an indigenous computer manufacturing capability, the government forced consolidation through mergers of the existing firms (as discussed in these pages) with the hope that at least a single firm would succeed. Ultimately, International Computing Limited (ICL) was this firm, but it eventually succumbed to substantial pressure from American computer vendors.

ICL was acquired by Fujitsu in the mid-1990s. With its acquisition, the indigenous British computer manufacturing capability disappeared. It was an unfitting end to a capability that led the way in the early days of computer development.

CHAPTER ONE

MARCONI ELLIOTT COMPUTER SYSTEMS

Source: CCS 2015j

Marconi Elliott Computer Systems (MECS) emerged from the merger of Marconi, GEC, AEI, and Elliott Automation in 1968. After 1971, it renamed itself GEC Computers Ltd.

Marconi Elliott continued development of the English Electric 2xxx and Elliott Automation 9xx series of computing machines. In 1970 they announced the "New Range" of computing machines tentatively titled the "alpha", "beta", and "gamma" machines. However, when Marconi Elliott was renamed GEC Computers, the "alpha" was relabeled the GEC 2050 and the "beta" as the GEC 4080. The "gamma", planned as a 32-bit computer was never built, but some its features were incorporated into the GEC 4080.

Eventually, MECS was dismembered with the major elements transferred to a new company, International Computers, Ltd. The remaining elements were eventually renamed GEC Computers, Ltd., which is discussed in Chapter Two.

Ferranti was financially strong for a while enough to continue development of several computers because if its diverse array of businesses. Eventually, it to transferred its computing division to GEC although the company continued in business until the early 1990s.

Marconi Electronic Systems, comprising the defence-related business, was sold to British aerospace in 1999, which eventually was renamed BAE Systems. Thus passed a historic name in British industry into history.

1.1 MARCONI – THE EARLY YEARS

Marconi Company arose from the pioneering work in radio transmission by Guglielmo Giovanni Maria Marconi

Guglielmo Giovanni Maria Marconi (1874-1937)

Guglielmo Marconi was an Italian inventor and electrical engineer, who created the practical wireless telegraph system, known as "radio". He was born in 1874 in Bologna, Italy. From an early age, he was tutored at home in chemistry, mathematics, and physics. By the age of 18, he was attending lectures at the University of Bologna and using its laboratories and library under Augusto Righi. By the early 1890s, he was investigating electromagnetic radiation, then known as Hertzian Waves (radio waves), which induced him to explore wireless telegraphy based on radio waves, which did not seem to interest other researchers.

In 1894, he demonstrated a radio transmitter and receiver to is mother, which made a bell ring on the other side of a room at the push of a button. From this work, he developed numerous devices that could work over long distances. He developed a functional system with an oscillator, a coherer receiver, a telegraph key, and a telegraph received. Through the 1890s and early 1900s, he demonstrated many systems in England with connections to the United States and Canada.

In 1897, he had established The Wireless Telegraph and Signal Company in the United Kingdom in 1897. The role of wireless telegraphy in the Titanic tragedy significantly raised public awareness.

By this time, it had been renamed the Marconi Company and branched out in many areas based on its work in continuous wave transmissions which were used for audio transmissions. In 1909 he was awarded half of the Nobel Prize for contributions of the development of wireless telegraphy.

Marconi eventually died of a ninth heart attack on 20 July 1937. The Marconi Company survives to this day as an innovator in electronics and communication.

1.1.1 MARCONI TAC

Source: MCL 1960sg, CCS 2020k

Marconi began experimenting with computers in 1959 to supports its development of processing systems for radar systems – a prime focus of the company for many years. Their first system was the Marconi Transistorized Automatic Computer (TAC) of which seven may have been built (CCS)

2020k). A pair of machines was installed at the Wylfa Nuclear Power Station on Anglesey, UK to monitor its nuclear reactors. These machines ran for 38 years until they were switched off in 2004. One machine of the pair is owned by The National Museum of Computing (TNMOC) at Bletchley Park, where it has been restored (CCS 2020k). Figure 1-1 depicts the TNMOC's TAC. Figure 1-2 depicts operator console of the TAC.



Figure 1-1. TNMOC Marconi TAC Source: Courtesy of TNMOC 2024



Figure 1-2. TAC Operator Console Source: Courtesy of MCL 1960sg

The Marconi TAC's characteristics are presented in Table 1-1.

Table 1-1 Marconi TAC – Basic Characteristics

Characteristic	Value/Explanation
Internal Representation	Fixed Point Binary
# Bits/Word	20
# Instructions/Word	1
# Instructions	
# Bits/Instruction	20
Instruction Type	Single Address
CPU Technology	Diode Transistor Logic; Germanium Junction
	Transistors
CPU Registers	
Main Memory	Magnetic Core: 4K words, Access: 10 usecs
Add Time	Fixed Point: 22 usecs
Multiply Time	Fixed Point: 92 usecs
Divide Time	N/A

The TAC was one of the first microcoded machines developed in Europe.

The input facility was a paper tape reader and the output facility was a Friden Flexowriter typewriter.

Optional peripheral devices included a magnetic drum and a display unit. Figure 1-3 depicts the TAC cabinets.

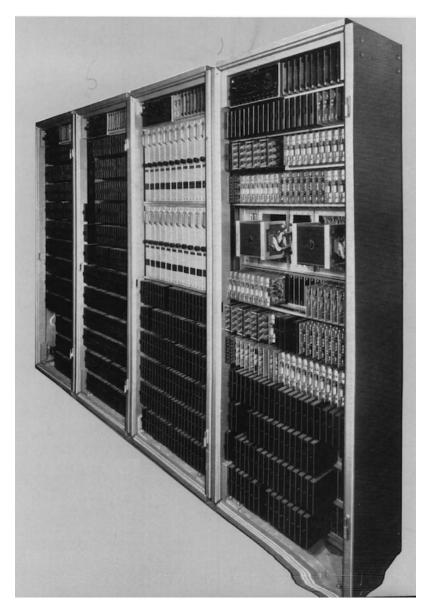


Figure 1-3. Marconi TAC Source: Courtesy of CCS 2020k

Multiple images of a Marconi TAC are depicted at the Jim Austin collection at

 $https://www.computermuseum.org.uk/fixed_pages/marconi_TAC.html.$

1.1.2 THE IMP

The High-Speed Miniature Processor (IMP) was a prototype for the first general-purpose computer developed by Marconi Computers Limited. Figure 1-4 depicts the IMP with John Keene and Peter Jeffries.



Figure 1-4. IMP Prototype Source: MCL circa1964e

When it was fully assembled and operational, it was deemed successful and capable, so the IMP team was asked to design a commercial version, which was named the Myriad. Many of the core components (circuit board, power supplies, and cabinetry) were redesigned (CCS 2020k).

1.2 THE MYRIAD FAMILY

Source: Marconi 1966c, Wikipedia 2023

Based on its work in radio transmissions, the Marconi Company developed the Myriad computer family beginning in the mid-1960s. It was so named because Marconi believed that it would have a "myriad" of applications. The Myriad family machines were used by several nations, including Britain's Royal Radar Establishment (RRE) and Sweden in their "Fur Hat" defence system. Two Myriad systems were used by the Royal Air Force for meteorological analysis (Wikipedia 2024).

1.2.1 Myriad I

Source: MCL 1968a, Wikipedia 2023

The Myriad I was designed as a conventional computer in a small desk format. It weighed about 1220 pounds. Standard input was provided by paper tape readers, which the software handled either as ASCII or the KDF9 character codes. First deliveries were in 1965. Standard output was provided by a high-speed line printer.

An interesting feature was that the Myriad 1 was built with a battery backup to handle short-term power failures.

Table 1-2. Myriad I – Basic Characteristics

Characteristic	Value/Explanation
Internal Representation	Fixed Point Binary
# Bits/Word	24
# Instructions/Word	1
# Instructions	52 (possible 64 order codes)
# Bits/Instruction	24
Instruction Type	Single Address
CPU Technology	Integrated circuits, diode transistor logic (DTL)
CPU Registers	A, B (24 bits)