Designing Analog Switches

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By

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Dedicated to my loving wife
S. Latha (late)

CONTENTS

PREFACE

The most popular analog switch ICs CD4066 and DG 201 are used for many electronic circuits. This book explains how they are used for (i) analog function circuits and (ii) digital circuits.

I am highly indebted to my

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CHAPTER 1

INTRODUCTION TO ANALOG SWITCHES

An analog switch (or a "switch") is a switching device capable of switching or routing analog signals which can have any level within a specified legal range, based on the level of a digital control signal. Commonly implemented using a "transmission gate," an analog switch performs a function similar to that of a relay. For example, an analog switch can turn an audio signal on or off based on a MUTE signal; or analog switches could send one of two signals to a headphone amplifier. They are most commonly implemented using CMOS technology integrated circuits.

1.1 Transistor Switches

Figure 1.1 shows simple transistor shunt switch. Let V_C = HIGH($+V_{CC}$), the transistor base emitter terminals are forward biased and hence it is ON.

V_{BE} = 0.7V for silicon transistor and 0.3V for germanium transistor,

$$V_{CE} \approx O\ V$$

$$I_C = \frac{V_1}{R_C}$$

$$I_C = \beta I_B$$

$$V_O \simeq OV$$

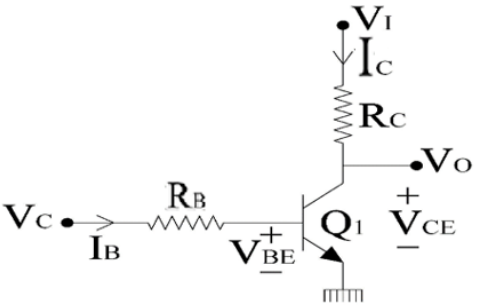

Fig. 1.1 transistor shunt switch

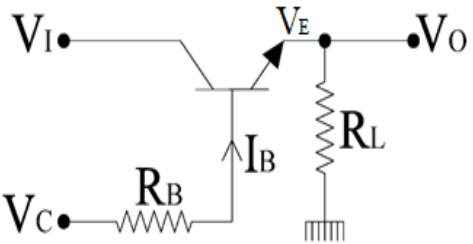

Fig. 1.2 transistor series switch

Let V_C = LOW ($-V_{CC}$), the transistor base emitter terminals are reverse biased and hence it is OFF,

$I_B = O$

$V_{CE} \approx V_I$

$I_C = O$

$V_O \simeq V_{CE} = V_I$

From the above it is understood that when control input V_C is HIGH, output voltage is zero volts and when control input V_C is LOW, the output voltage is approximately equal to input voltage.

Figure 1.2 shows a transistor series switch. If control input V_C is HIGH (+ V_{CC}), transistor base emitter junction is forward biased and it is ON,

$V_E \simeq V_I$

$V_O = V_I$

Next, if control input V_C is LOW ($-V_{CC}$), transistor's base emitter junction is reverse biased and hence it is OFF,

$I_B = O$

$V_E \neq V_I$

$V_O = O$

From the above discussions, it is understood that when control input V_C is HIGH, the transistor is ON and output voltage is the input voltage. When control input V_C is LOW, the transistor is OFF and the output voltage is zero volts.

1.2 Jfet Switches

Fig. 1.3(a) shows Junction Field Effect Transistor (JFET) as a series switch. If control input is HIGH($+V_{CC}$), zero volts will exist on gate terminal, JFET is ON and acts as a closed switch. OUT ~ IN. If the control input CON is LOW($-V_{CC}$), negative voltage will exist on gate terminal, JFET is OFF and acts as an open switch. OUT ~ 0.

Fig. 1.3(b) shows a JFET shunt switching circuit. If control input CON is HIGH(+Vcc), zero volts will exist on gate, FET is ON and zero volts will be the output. OUT ~ 0. If the control input CON is LOW($-V_{CC}$), negative voltage will exist on gate terminal, the FET operated on cut-off region and acts as an open circuit. The output will be OUT ~ IN.

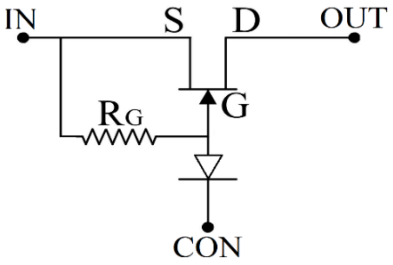

Fig. 1.3(a) JFET series switch

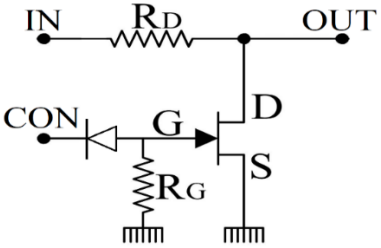

Fig. 1.3(b) JFET shunt switch

1.3 Mosfet Switches

Fig. 1.4(a) shows a MOSFET series switch. If the control input is HIGH($+V_{DD}$), the channel resistance becomes very small and allows maximum drain current to flow. This is the saturation mode and the MOSFET is completely ON and acts as a closed circuit OUT ~ IN. If the control input is LOW(V_{SS}), the channel resistance becomes HIGH and no current flows from drain. This is a cut off region and MOSFET is completely OFF and acts as an open switch. OUT ~ 0.

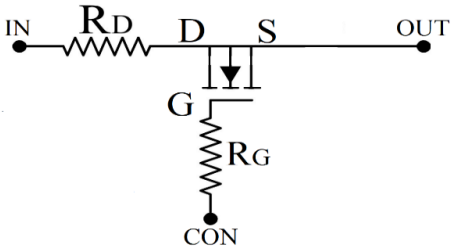

Fig. 1.4(a) MOSFET series switch

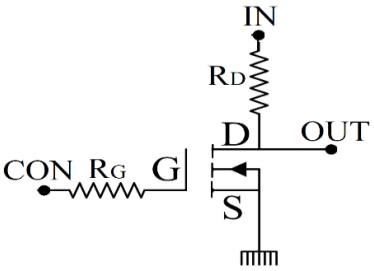

Fig. 1.4(b) shows a MOSFET shunt switch. If the control input is HIGH($+V_{DD}$), the channel resistance becomes very small and allows maximum drain current to flow. This is the saturation mode and the MOSFET is completely ON and acts as a closed circuit. OUT ~ 0. If the control input is LOW(V_{SS}), the channel resistance becomes HIGH and no current flows from the drain. This is a cut off region and MOSFET is completely OFF and acts as an open switch. OUT ~ IN.

1.4 CD 4066

The symbol of an analogue switch is shown in Fig. 1.5. It has three terminals, CON, IN/OUT and OUT/IN. If control (CON) pin is LOW, the switch S_1 is opened so that IN/OUT and OUT/IN terminals are disconnected. If the control (CON) pin is HIGH, the switch S_1 is closed so that IN/OUT and OUT/IN terminals are connected together. Analog switches are available in an IC PACKAGE of CMOS CD4066 IC. The pin details of this CD4066 IC are given in Fig. 1.6.

It has three terminals, CON, IN/OUT and OUT/IN. If control (CON) pin is HIGH, the switch S_1 is opened so that IN/OUT and OUT/IN terminals are disconnected. If the control (CON) pin is LOW, the switch S_1 is closed so that IN/OUT and OUT/IN terminals are connected.

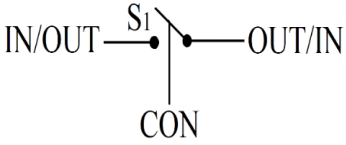

Fig. 1.5 non-inverted controlled switch symbol

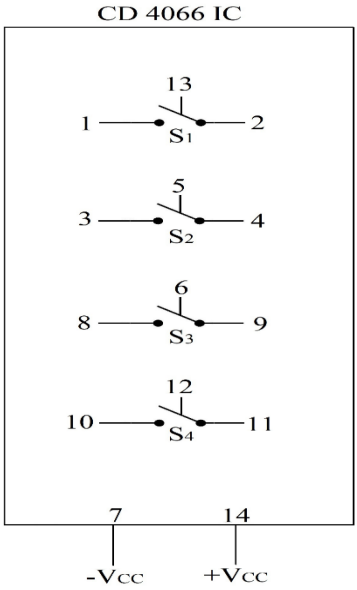

Fig. 1.6 pin details of CD 4066 IC

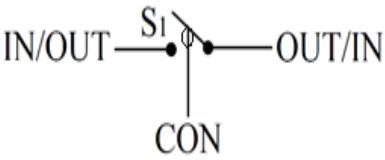

Fig. 1.7 inverted controlled switch symbol

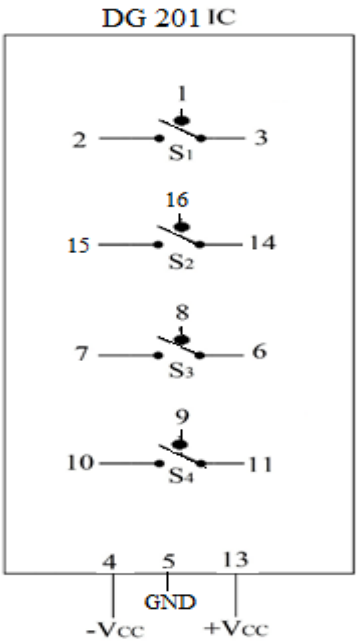

Fig. 1.8 pin details of DG201 IC

1.5 DG 201

The symbol of an inverted controlled analogue switch is shown in Fig. 1.7. Inverted controlled analogue switches are available in an IC PACKAGE of DG201 IC. The pin details of this DG201 IC are given in Fig. 1.8.

1.6 555 Timer

555 Timer is a highly stable IC for generating accurate time delay or oscillation. The IC 556 contains two 555 timers and is a 16 pin DIP IC. 555 is 8 pin DIP IC. Its pin detail is shown in Figure. 1.9. 555 timer will provide time delay ranging from microseconds to hours.

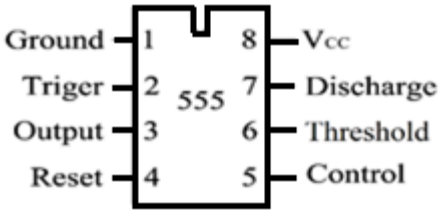

Fig. 1.9 Pin details of 555 timer

Meanings of Pin Connections of IC 555

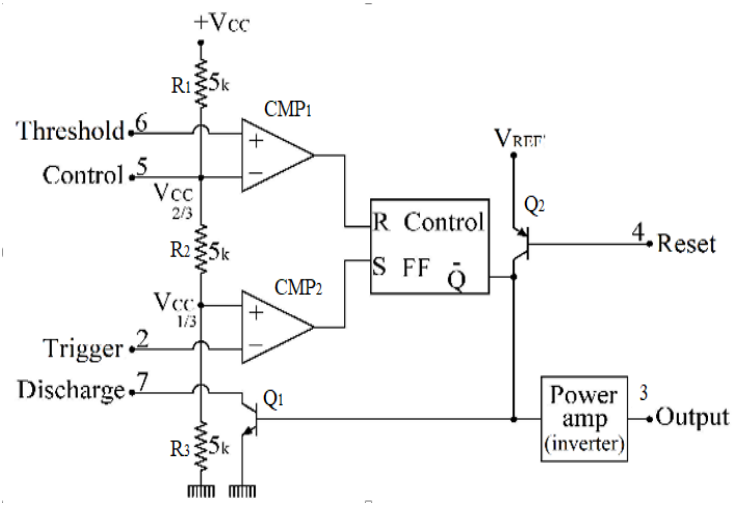

Fig. 1.10 Functional diagram of 555 timer

Figure 1.10 shows functional diagram of 555 timer. The resistors R_1, R_2 and R_3 are used as voltage divider and provides voltage reference (i) $\frac{2}{3}V_{CC}$ for upper comparator CMP_1 and (ii) $\frac{1}{3}V_{CC}$ for lower comparator CMP_2. Initially when the power supply switch is on, the output of upper comparator CMP_1 will be LOW, i.e. R = 0, the output of lower comparator CMP_2 will be HIGH, i.e. S = 1. The flip flop outputs are Q = 1 and Q' = 0. The timer

output at pin 3 will be HIGH, transistor Q_1 is OFF and hence the discharge pin 7 is at open position. Let the threshold pin 6 and trigger pin 2 be tied together and a rising voltage is applied to these connected pins 2 and 6. When the rising voltage is increased above $2V_{CC}/3$, the output of upper comparator CMP_1 becomes HIGH, i.e. R = 1, the output of lower comparator CMP_2 becomes LOW, i.e. S = 0. The flip flop outputs are Q = 0 and Q' = 1. The timer output at pin 3 will be LOW, transistor Q_1 is ON and hence the discharge pin 7 is at GND potential. Now let us change the rising voltage into falling voltage and when falling voltage goes below 1/3 V_{CC}, the output of upper comparator CMP_1 becomes LOW, i.e. R = 0, the output of lower comparator CMP_2 becomes HIGH, i.e. S = 1. The flip flop outputs are Q = 1 and Q' = 0. The timer output at pin 3 will be HIGH, transistor Q_1 is OFF and hence the discharge pin 7 is at open position. The reset pin 4 is used to reset the flip flop if there are any overrides in the operation. The transistor Q_2 is working as a buffer to isolate the reset input from flip flop and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{REF} obtained from V_{CC}. The different operation states of 555 timer are shown in Table I.

CHAPTER 2

WAVEFORM GENERATORS

The circuits which generate sine, square, pulse, saw tooth and triangular waveforms are discussed in this chapter. These waveforms are used in timing and control, signal carriers for information transmission and storage, sweep signals for information display, test signals for automatic test and measurement and audio signals for electronic music. The function of function generator is to produce a waveform of a particular frequency, amplitude, and shape and duty cycle. Sine wave oscillators are used to test the characteristics of low pass, high pass and band pass filters. Pulse waveforms are used to test digital circuits. Saw tooth and triangular waves are required to develop function circuits either internally or externally.

2.1 Astable Multivibrator

Fig. 2.1 shows an astable multivibrator using op-amp. Let us assume initially op-amp output is LOW (i.e. negative saturation). The voltage at non-inverting terminal will be,

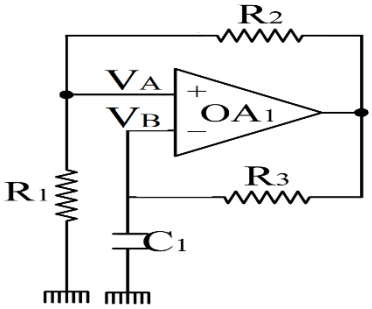

Fig. 2.1 astable multivibrator

$$V_A = \beta(-V_{SAT})$$

$$\beta = \frac{R_1}{R_1 + R_2} \tag{2.1}$$

The voltage at inverting terminal V_B will be positive w.r.t V_A and its potential is decreasing, i.e. C_1 charges down through R_3. When potential difference between the two input terminals approaches zero, the op-amp comes out of saturation. The positive feedback from the output to terminal V_A causes regenerative switching which drives the op-amp to positive saturation. Capacitor C_1 charges up through R_3 and V_B potential rises exponentially; when it reaches $V_B = \beta(+Vcc)$ the circuit switches back to the state in which op-amp is in negative saturation. The sequence therefore repeats to produce square waveform of time period T at its output. The time period T is given as,

$$T = 2R_3C_1 \ln(1 + 2\frac{R_1}{R_2}) \tag{2.2}$$

Voltage to period converter: If in the astable multivibrator shown in Fig. 2.1, the R_2 terminal is removed from the output terminal and analog switches S_1-S_2 are added between R_2 and output as shown in Fig. 2.2, then the circuit will work as voltage to time period converter. The time period T is given as,

$$T = V_I K_1 \tag{2.3}$$

Where K_1 is a constant depends on equation (2.2) and op-amp saturation voltage or supply voltage Vcc.

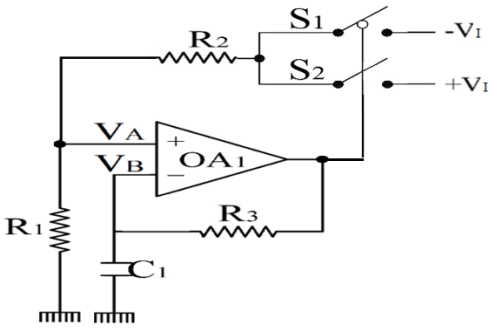

Fig. 2.2 voltage to period converter

Voltage to frequency converter: If in the astable multivibrator shown in Fig. 2.1, the R_3 terminal is removed from the output terminal and analog switches S_1-S_2 are added between R_3 and output as shown in Fig. 2.3, then the circuit will work as a voltage to frequency converter. The frequency 'f' is given as,

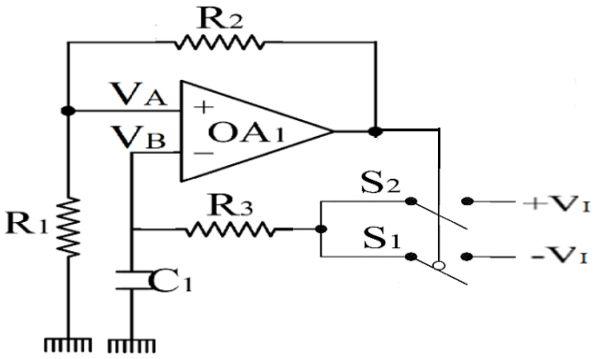

Fig. 2.3 voltage to frequency converter

$$f = V_I K_1 \tag{2.4}$$

Where K_1 is a constant depends on equation (2.2) and op-amp saturation voltage or supply voltage V_{CC}.

2.2 Saw Tooth Wave Generators

Two circuits for generation of saw tooth wave are shown in Fig. 2.4 and their associated waveforms in Fig. 2.5. A saw tooth wave V_{S1} of peak value V_R and time period T is generated by these circuits.

In Fig. 2.4(a)

$$V_R = 2V_{BE} \tag{2.5}$$

$$T = 1.4R_1C_1 \tag{2.6}$$

In Fig. 2.4(b), if initially op amp OA_2 output is LOW, the switch S_1 is opened and the integrator formed by resister R_1, capacitor C_1 and op amp OA_1 integrates ($-V_R$) and its output is given as,

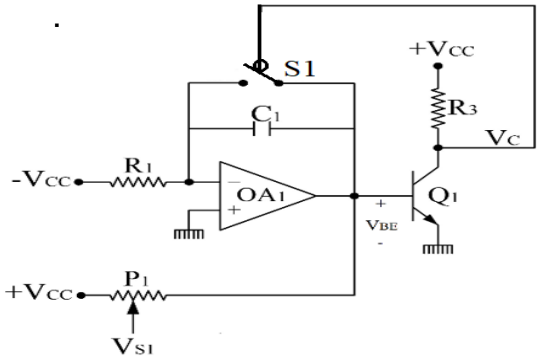

Fig. 2.4(a) Saw tooth wave generator – I

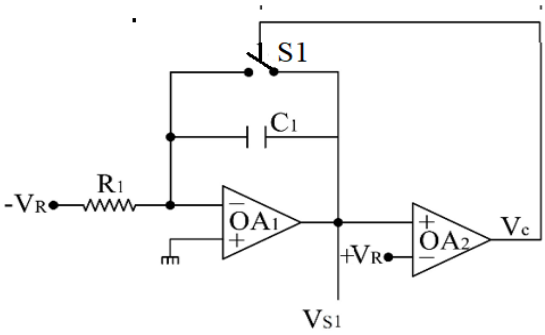

Fig. 2.4(b) Saw tooth wave generator – II

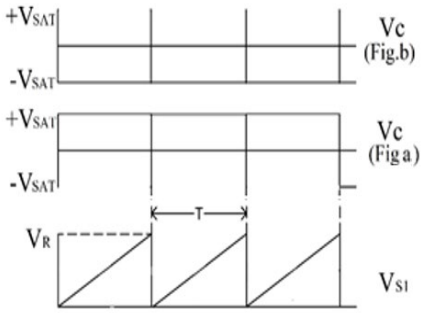

Fig. 2.5 Associated waveforms of Fig. 2.4

$$V_{S1} = -\frac{1}{R_1 C_1}\int -V_R dt$$

$$V_{S1} = \frac{V_R}{R_1 C_1} t \tag{2.7}$$

A positive going ramp is generated at the output of op amp OA_1 and when it reaches the value of reference voltage $+V_R$ the comparator OA_2 output becomes HIGH. The switch S_1 is closed and shorts capacitor C_1 and hence integrator output becomes zero. Then comparator output is LOW and the sequence therefore repeats to give a perfect saw tooth wave V_{S1} of peak value V_R at the output of op – amp OA_1. From equation (2.7), Fig. 2.5 and the fact that at t= T, $V_{S1} = V_R$.

$$V_R = \frac{V_R}{R_1 C_1} T$$

$$T = R_1 C_1 \tag{2.8}$$

2.3 Function Generator – Type I

A triangular wave V_{T1} with $\pm V_T$ peak to peak value and time period T is generated by the triangular wave generator shown in Fig. 2.6 and its associated waveforms are shown in Fig. 2.7.

The output of op amp OA_1 is a triangular wave V_{T1} with $\pm V_T$ peak values and time period of T. Let initially the comparator OA_2 output be LOW($-V_{SAT}$), the output of integrator composed by op-amp OA_1, resistor R_1 and capacitor C_1, is given as,

$$V_{T1} = -\frac{1}{R_1 C_1}\int -V_{SAT} dt = \frac{V_{SAT}}{R_1 C_1} t \tag{2.9}$$

The integrator output is rising towards positive saturation and when it reaches a value $+V_T$, the comparator output becomes HIGH($+V_{SAT}$). The output of integrator composed by op-amp OA_1, resistor R_1 and capacitor C_1, is given as,

$$V_{T1} = -\frac{1}{R_1 C_1}\int +V_{SAT} dt = -\frac{V_{SAT}}{R_1 C_1} t$$

Now the output of integrator is changing its slope from $+V_T$ towards $(-V_T)$ and when it reaches a value '$-V_T$', the comparator output becomes LOW($-V_{SAT}$) and the sequence therefore repeats to give (i) a triangular waveform V_{T1} with $\pm V_T$ peak to peak values at the output of op-amp OA_1 and (ii) a square waveform V_C with $\pm V_{SAT}$ peak to peak values at the output of comparator OA_2.

From the waveforms shown in Fig. 2.7, from equation (2.9) and the fact that at t = T/2, $V_{T1} = 2V_T$

$$2V_T = \frac{V_{SAT}}{R_1 C_1}\frac{T}{2}$$

$$T = \frac{4V_T R_1 C_1}{V_{SAT}} \tag{2.10}$$

When the comparator OA_2 output is LOW ($-V_{SAT}$), the effective voltage at non-inverting terminal of comparator OA_2 will be by superposition principle,

$$\frac{(-V_{SAT})}{(R_2 + R_3)}R_2 + \frac{(+V_T)}{(R_2 + R_3)}R_3$$

When this effective voltage at non-inverting terminal of comparator OA_2 becomes zero,

$$\frac{(-V_{SAT})R_2 + (+V_T)R_3}{(R_2 + R_3)} = 0$$

$$(+V_T) = (+V_{SAT})\frac{R_2}{R_3}$$

When the comparator OA_2 output is HIGH($+V_{SAT}$), the effective voltage at non-inverting terminal of comparator OA_2 will be by superposition principle,

$$\frac{(+V_{SAT})}{(R_2 + R_3)}R_2 + \frac{(-V_T)}{(R_2 + R_3)}R_3$$

When this effective voltage at non-inverting terminal of comparator OA_2 becomes zero,

$$\frac{(+V_{SAT})R_2 + (-V_T)R_3}{(R_2 + R_3)} = 0$$

$$(-V_T) = (-V_{SAT})\frac{R_2}{R_3}$$

$$\pm V_T = \pm V_{SAT}\frac{R_2}{R_3} \approx 0.76(\pm V_{CC})\frac{R_2}{R_3}$$

(2.11)

From equation (2.10) and (2.11), time period T of the generated triangular/square waveforms is given as,

$$T = 4R_1C_1\frac{R_2}{R_3} \tag{2.12}$$

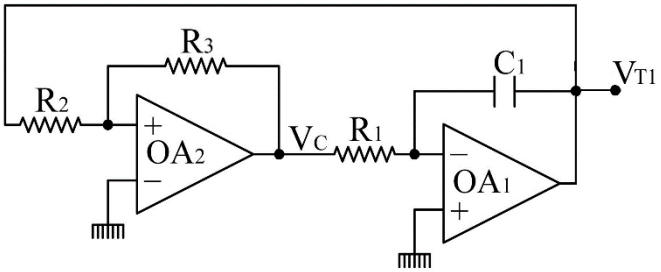

Fig. 2.6 triangular wave generator

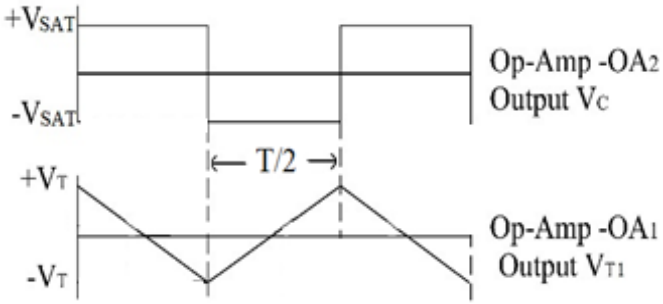

Fig. 2.7 associated waveforms of Fig. 2.6

The triangular wave generator shown in Fig. 2.6 can be converted into voltage-controlled function generator by adding an analog switch between comparator and integrator as shown in Fig. 2.8.

$$T = \frac{4V_T R_1 C_1}{V_I} \tag{2.23}$$

$$T = \frac{4R_1 C_1}{V_I}\frac{R_2}{R_3} \tag{2.24}$$

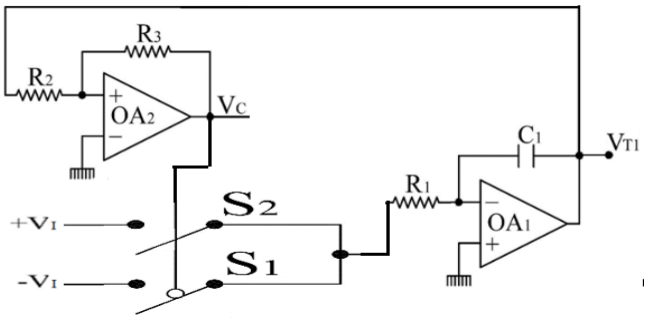

Fig. 2.8 Function Generator

2.4 Function Generator – Type II

The circuit diagram of the function generator – type II is shown in Fig. 2.9 and its associated waveforms are shown in Fig. 2.10.

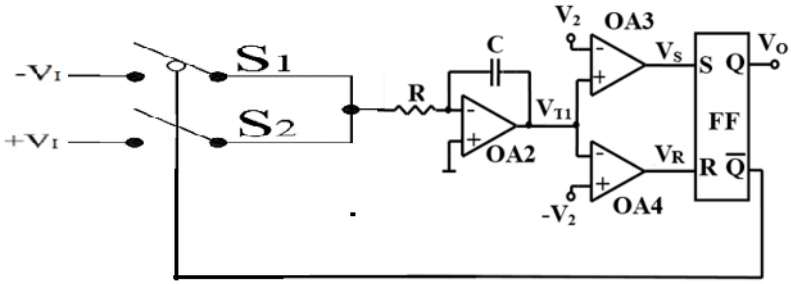

Fig. 2.9

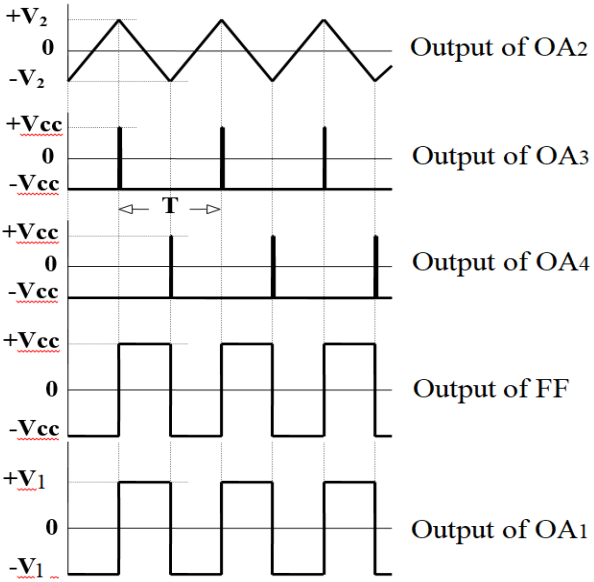

Fig. 2.10 Associated Waveforms of Fig. 2.9

Let initially the SR flip flop output Q be LOW. The switches S_1-S_2 select $-V_1$ (switches S1 is closed and S2 is opened). $-V_1$ will be given to the integrator formed by OA_2, resistor R and capacitor C. Its output will be,

$$V_{T1} = -\frac{1}{RC}\int -V_1 dt = \frac{V_1}{RC}t \qquad (2.25)$$

The output of integrator OA2 is a positive going ramp. When the output of the integrator exceeds the other input voltage V_2, SR Flip flop output Q is set to HIGH by the comparator OA_3. The switches S_1-S_2 select $+V_1$ (switches S1 is opened and S2 is closed) and $+V_1$ is given to the integrator OA_2. Now the integrator output will be,

$$V_{T1} = -\frac{1}{RC}\int V_1 dt = -\frac{V_1}{RC}t \tag{2.26}$$

The output of integrator is changing its slope from positive to negative. When the output of the integrator exceeds the input voltage $-V_2$, SR flip flop output 'Q' will be reset to LOW by the comparator OA_4 and the cycle therefore repeats. From the equation (2.26) and from the waveforms shown in Fig. 2.10 at t = T/2, $V_T(t) = 2V_2$

$$2V_2 = \frac{V_1}{2RC}T \tag{2.27}$$

$$T = \frac{V_2}{V_1}4RC \quad , \quad f = \frac{V_1}{V_2}\frac{1}{4RC} \tag{2.28}$$

Worked Examples

2.1 Design a square wave generator for frequency of 1KHz. Power supply voltage of ±15V.

The square wave generator or astable multivibrator is given in Fig. 2.1. From equation (2.2),

$$T = 2R_3C_1 \ln(1 + 2\frac{R_1}{R_2})$$

Given; frequency = 1kHz

T = 1/f = 1mS

Let $R_2 = 1.16R_1$

Let R_1 = 10K, then R_2 = 11.6K

$$T = 2R_3C_1 \ln 2.7241 = 2R_3C_1$$

$$R_3 = \frac{T}{2C_1}$$

Let $C_1 = 0.05\mu F$,

$$R_3 = \frac{1X10^{-3}}{2X0.05X10^{-6}} = 10K$$

2.2 Design a saw tooth wave generator with peak value of 5V and time period of 1mS.

The saw tooth wave generator is shown in Fig. 2.5. Choose $V_R = 5V$ with LM3365V reference diode. Given: T = 1mS. Let $R_1 = 1M$.

From equation (2.8)

$$T = R_1C_1, \quad C_1 = \frac{T}{R_1} = \frac{1X10^{-3}}{1X10^6} = 1nF$$