Simulation and Modeling of Emerging Devices

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Tunnel Field-Effect and Fin Field Effect Transistors

By

Brinda Bhowmick, Rupam Goswami and Rajesh Saha

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Symbol	Description	Symbol	Description
V_{DS}	Drain to source voltage	k	Boltzmann constant
V_{GS}	Gate to source voltage	I_{on}	On current
V_G	Gate voltage	I_{off}	Off current
V_{FB}	Flat band voltage	x	Mole fraction, Position
E_g	Band gap energy	E_c	Conduction Energy
I_D	Drain current	C_L	Load Capacitance
V_T, V_{th}	Threshold voltage	SS	Subthreshold swing
L, L_g	Channel length	$\sigma V_T, \sigma V_{th}$	Variation in threshold voltage
E	Electron wave energy	σSS	Variation in subthreshold swing
$\psi_{S,\min}$	Minimum surface potential	σI_{on}	Variation in on current
ψ_s	Surface Potential	σI_{off}	Variation in off current
T_{fin}	Fin thickness	$\sigma\left(I_{on}/I_{off}\right)$	Variation in current ratio
H_{fin}	Fin height	NM_H	High state noise margin
t_{ox}	Oxide thickness	NM_L	Low state noise margin
L, L_g	Gate/channel length	$\overline{\phi}$	Average grain size
Ω	Wave function	Q_{inv}	Inversion charge

1

INTRODUCTION

1.1 Introduction

To get increased packing density, the dimensions of devices are reduced. Smaller device size enables higher device density in an integrated circuit. Hence the scaling down of the dimensions of MOSFETs (metal–oxide–semiconductor field-effect transistors) has been a continuous trend since their inception. As devices are scaled down, the influences from side regions and leakage currents become significant. Therefore, device long-channel approximations are no longer valid. In long-channel devices, the influence of electric fields emanating from the source/drain regions are much less important than those coming from the gate, since the center of the channel is far from the source/drain region, and the edge of the channel is only a small portion of the intrinsic part of the device. However, it is well known that this is no longer valid for devices with present-day technologies. To calculate the threshold voltage in these cases, the full multidimensional charge balance must be considered. This can have a significant impact on the threshold voltage values. In practice, short-channel effects (SCEs) provide the lower limit of achievable channel lengths for a given technology. SCEs tend to lower the threshold voltage for short-channel devices. This leads to larger I_{OFF} and higher power consumption.

This introductory chapter gives a brief outline of the SCEs in MOSFETs.

1.2 Short-Channel Effects

Various important SCEs in MOS transistors are channel-length modulation, threshold voltage roll-off, drain-induced barrier lowering (DIBL), bulk punchthrough, tunneling leakage currents, and velocity saturation.

Channel-length Modulation

Channel-length modulation in a MOSFET is the first of all SCEs historically observed. It is due to the increase of the depletion layer width at the drain with increased drain voltage [1]. This leads to a shorter channel length and an increased drain current (Fig. 1.1). The channel-length-modulation effect typically increases in small devices with low-doped substrates. An extreme case of channel-length modulation is punchthrough, where the channel length reduces to zero. Proper scaling can reduce channel-length modulation, namely by increasing the doping density as the gate length reduces [1].

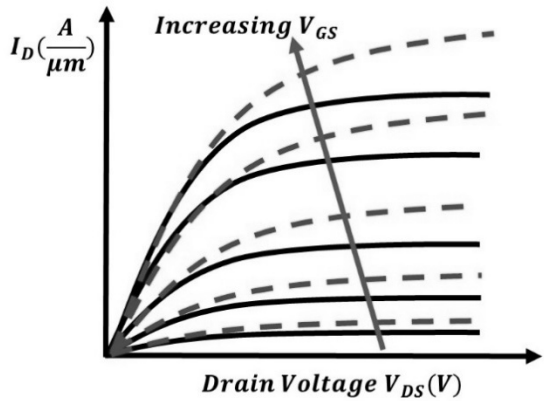

FIGURE 1.1 Current-voltage characteristics of a MOSFET with (dotted) and without (solid) channel-length modulation for different gate voltages

Threshold Voltage Roll-off

When the edge effects are enhanced, the depletion width for the drain junction is almost equal to that for the source junction. Since the channel-depletion region overlaps the source and the drain-depletion regions, the charge induced by the gate bias field can be approximated within the

trapezoidal region as shown in Fig. 1.2. The threshold roll-off is given by [2],

$$\Delta V_T = \frac{qN_A W_m r_j}{C_{ox} L}\left[\sqrt{1+\frac{2W_m}{r_j}} - 1\right]$$

Where N_A is the acceptor concentration, W_m is maximum depletion width, C_{ox} is oxide capacitance, q is the electron charge and r_j is the junction depth.

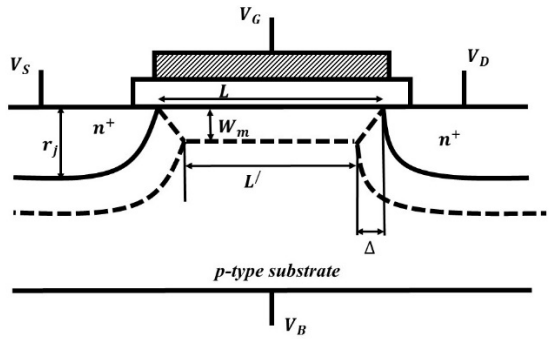

FIGURE 1.2 Two-dimensional schematic of a MOSFET showing the parameters responsible for threshold voltage roll-off

Drain-Induced Barrier Lowering

When the gate voltage is below the threshold voltage V_T, the p-Si substrate forms a potential barrier between n+ source and drain. For short-channel devices, the applied potential at the drain pulls down this barrier. This effect becomes more prominent when the device works in the saturation region due to a large drain voltage with a significantly wider drain junction depletion layer depth. This barrier lowering effect leads to a substantial increase in electron injection from source to the drain, resulting in an enhanced drain current [3]. This effectively reduces the threshold voltage further. With the increase of drain voltage, the conduction band energy is lowered as observed in Fig. 1.3. The threshold voltage roll-off is seen for around 2 μm gate length. The change in drain voltage causes the variation in threshold voltage for short-channel devices as shown in Fig. 1.4.

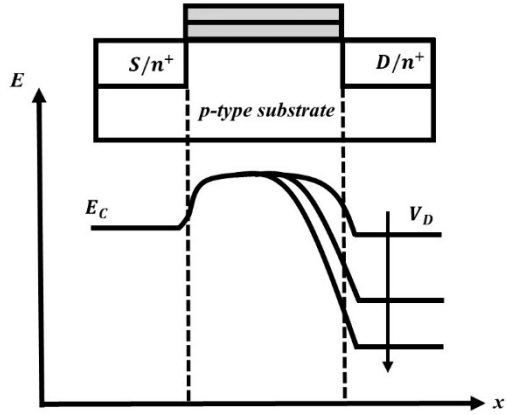

FIGURE 1.3 Effect of Drain induced Barrier Lowering on conduction band edge

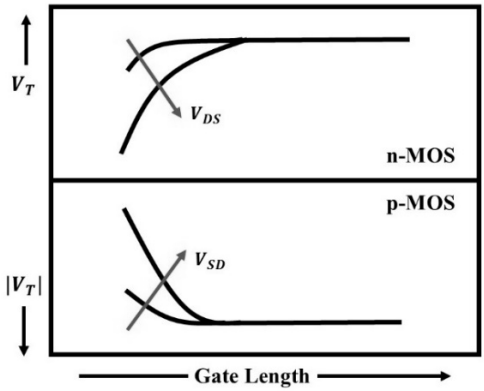

FIGURE 1.4 Threshold voltage roll-off with gate length

Bulk Punchthrough

If the drain voltage is large enough, a significant amount of leakage current flows from drain to source via the bulk of the substrate in a short-channel MOSFET. The gate can no longer turn the device completely off and loses its control over the channel [4, 5]. Moreover, high leakage current limits device performance for short-channel MOSFETs, as shown in Fig. 1.5.

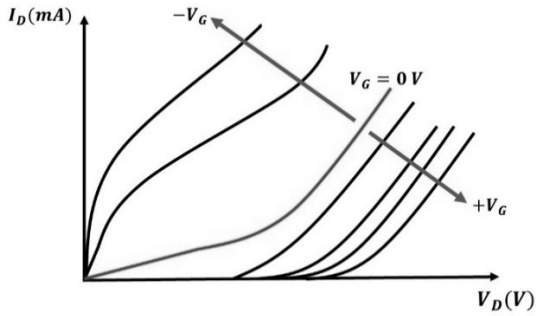

FIGURE 1.5 Effect of punchthrough

Tunneling Leakage Currents

Quantum mechanical tunneling of carriers through the energy barriers in the device is another limiting factor for the scaling of the MOSFETs, as they increase the leakage currents significantly. Band-to-band (Zener) tunneling between body and drain, direct source-to-drain tunneling current and tunneling from the gate oxide are classified as the three major sources of tunneling leakage currents that come into effect as the device dimensions are scaled down [6, 7].

Leakage currents come primarily from two sources: gate oxide leakage and subthreshold leakage. Fig. 1.6 shows the gate oxide leakage that occurs when electrons jump (“tunnel”) from the gate to the channel through the gate oxide. Scaling reduces the thickness of the oxide and the thinner the oxide the higher is the leakage due to tunneling. Subthreshold leakage occurs when a nonzero channel current flows even in the absence of an inversion layer; that is, the gate voltage is below V_{th} when ideally the channel should be “off”. Subthreshold leakage becomes worse as V_{th} is lowered due to SCEs in scaled-down devices.

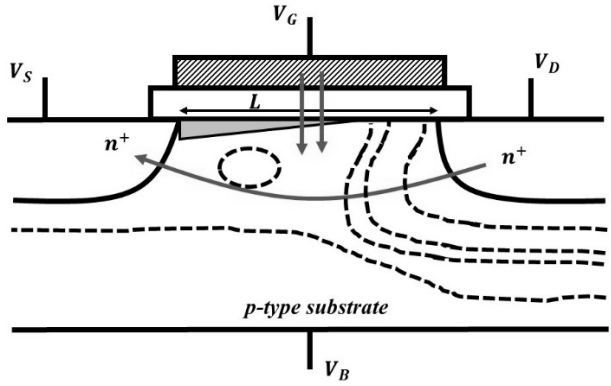

FIGURE 1.6 Tunneling leakage currents

Gate-Induced Drain Leakage Current

Due to the reduction of the MOSFET gate oxide thickness, the fields in both the oxide and silicon in the gate-drain overlap region increase. The large fields deplete the drain overlap region, leading to significant band bending. This leads to a band-to-band tunneling current in the gate-overlap, deep-depleted drain regions. This gate-induced drain leakage (GIDL) current has been well observed in conventional MOSFETs and seen as degradation of short-channel performance and leakage currents [8]. The GIDL current is strongly dependent on gate and drain bias. As the MOSFET channel length is scaled down, the nonscalability of the overlap region further degrades the device performance. The GIDL current, however, strongly depends on the doping profile of the drain. For very high drain doping, even though the depletion width is very narrow, the FERMI potential (E_F) gets pinned, which in turn prevents band bending at the oxide–silicon interface and hence suppresses the tunneling leakage currents. For low drain doping, even though the band bending is significant, the depletion width is too wide to cause any significant tunneling current. Therefore, the GIDL currents exist only within a certain doping range.

Gate Oxide Leakage Current

To minimize SCEs and maintain constant field in the oxide, in accordance with Dennard's scaling rule, the gate oxide thickness, t_{ox}, is scaled in proportion to L and *W*. However, as t_{ox} is scaled, tunneling leakage current

through the oxide comes into the picture and starts increasing [9, 10]. It has been shown that the silicon dioxide can be thinned down to slightly below 2 nm before the leakage currents are large enough to become unacceptable. The tunneling takes place not only in the inversion layer but also in the accumulation region, as well as the region where the gate overlaps the source and the drain. As a result, the latter component becomes significant in a scaled device. A possible solution to reduce the direct tunneling through the insulator is the use of physically thicker gate dielectric material with relative dielectric constant, $\mathcal{E}$, higher than that of silicon dioxide. However, the thickness cannot grow to an unlimited limit as two-dimensional effects in the thicker insulator start to interfere with scaling. Therefore, the short-channel performance is degraded due to the fringing fields from the source and the drain regions, which become non negligible as the thickness-to-length aspect ratio increases [11].

Velocity Saturation

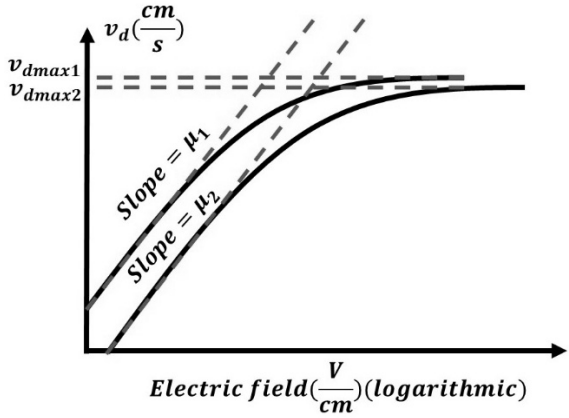

FIGURE 1.7 Velocity saturation effect is shown

In a short-channel device, the longitudinal electric field is no longer negligible compared to the transverse field. In terms of drain current under normal device operation, the most significant effect is the effective reduction of mobility with the increasing longitudinal field [12]. Fig. 1.7 illustrates the behavior of drift velocity v_d with electrical field (*E*). The velocity of carriers in the inversion layer tends to saturate at high *E* values.

Effects due to lack of proportionality between v_d and E on device characteristics are referred to as velocity saturation effects. In this regard, we have [12],

$$v_d \approx \mu|E|;\ |E| \leq E_c$$

$$\approx |v_d|_{max};\ |E| > E_c$$

and $E_c = \frac{|v_d|max}{\mu}$ where E_c is known as the critical electric field.

1.3 Scaling Rules in MOSFETs

As the device dimensions are miniaturized, the SCEs must be minimized to maintain device integrity. Some guidelines are required in scaled-device design. The term scaling denotes "the possibility of fabricating functional devices with equally good or even improved performance matrices but smaller physical dimensions" [13]. "One elegant approach for maintaining the long-channel behavior is to simply reduce all dimensions and voltages by a scaling factor α(>1), so that the internal electric fields are the same as those of a long-channel MOSFETs. This approach is called "constant field scaling". Scaling is also possible without making any change to the supply voltage [14]. Table 1.1 summarizes the scaling rules of constant-field scaling for various device parameters and circuit performance factors. The circuit performance, i.e., speed and power consumption in the on state, can be enhanced as the device dimensions are scaled down. In practical integrated circuit manufacturing, however, the electric fields inside the smaller devices are not kept constant but allowed to increase to some extent. This is mainly because the power supply and V_T cannot be scaled arbitrarily. If the threshold voltage is too small, the leakage level in the off state $(V_G = 0\,V)$ will increase significantly because of the nonscalable subthreshold swing. Consequently, standby power consumption will also increase. By applying the scaling rules, MOSFETs have been fabricated having channels as short as 20 nm, a very high transconductance (>1000) mS/mm), and reasonable subthreshold swing (120 mV/decade).

According to the two scaling strategies defined in Table 1.1, all the lateral (primarily the gate width and the length) and the vertical dimensions should decrease from one technology generation to the next by the factor α, thus yielding an increase of the number per unit chip area by the factor α^2. The constant field and constant supply voltage scaling rules are derived

from quite simple one-dimensional models of MOSFET electrostatics. These models and the rules became inadequate to the design of MOS transistors as the gate length (L_G) approaches one micron, thus leading to the development of more sophisticated criteria. As mentioned in Table 1.1 the mixed scaling is proposed in [15] to design 0.25μm MOSFETs, where different reduction factors are introduced for the geometrical dimensions (α) and the voltages (λ). Since the thermal voltage kT/q, the band and the junction built-in voltage do not scale, the subthreshold swing of the transfer characteristics and the flat band voltage of Poly-silicon gate MOSFET remain almost invariant to scaling [16]. As a result, the two-dimensional distribution of electrostatic potential inside the scaled device is distorted compared to that of the parent technology generation and so-called SCEs become apparent.

TABLE 1.1. Scaling rules for Complemenatry MOSFET (CMOS) technology

MOSFET device and circuit parameters	Constant field scenario	Constant voltage Scenario	Mixed scenario
Device dimensions (d,L,W,r_j)	1/α	1/α	1/α
Doping concentration (N_A, N_D)	α	α^2	α^2/λ
Voltage (V)	1/α	1	1/λ
Electric field (E)	1	α	α/λ
Current (I)	1/α	α	α/λ^2
Gate capacitance (C)	1/α	1/α	1/α
Oxide capacitance (C_{ox})	α	α	α
Interconnect resistance	α	α	α
Circuit delay time (τ)	1/α	$1/\alpha^2$	λ/α^2
Power dissipation per circuit(P)	$1/\alpha^2$	α	1
Power delay product per circuit (P, τ)	$1/\alpha^3$	1/α	$1/\alpha^2\lambda$
Power density (P/A)	1	α^3	α^3/λ^3

Note: α and λ denote the geometry and voltage scaling factors.

1.4 Control of SCEs in MOSFETs

An optimum choice of channel doping, the junction depth and the thickness of the gate dielectric is crucial to keep SCEs under control. Accurate tailoring of the source and drain extensions below the spacers and reduction of parasitic source/drain resistances contribute as well to achieving good performance and high I_{ON}/I_{OFF} ratios. As a consequence of the increased complexity of this optimization task, during the 1980s two- and three-dimensional CAD tools for numerical device simulation [17] found widespread use in the semiconductor industry to assist process engineers in analysis and tuning of the doping profiles to counteract SCEs. Studies on the scaling of CMOS technology have emerged from the joint efforts of associations such as the US Semiconductor Industry Association and, later, the International Technology Roadmap for Semiconductors (ITRS). The guidelines documents on MOSFET scaling prepared by the ITRS [18] aim at the early identification of risk factors in the development of the microelectronics industry.

Nowadays, the diversion of microelectronic applications has led to differentiation of the ITRS for high performance (HP), low power (LP) and low standby power (LSTP) [19]. Recently, all the roadmaps for the bulk MOSFET architecture have shared a common difficulty in finding the balance in the trade-off involving the containment of SCEs (which demands high channel doping and gate dielectrics with small equivalent oxide thickness (EOT)), the quest for high on current (which requires high carrier mobility and low threshold voltage), and the need for low subthreshold leakage (which requires high threshold voltage, low subthreshold, low subthreshold swing and relatively thick gate dielectrics). The performance matrices of bulk MOSFET technology have steadily improved. But for the channel-length sub 0.1µm range, it became increasingly difficult to maintain the historical scaling trends by mere optimization of the conventional architecture. The introduction of significant innovations has always been deferred till the time when no real alternative was possible due to complexity and cost. In this respect the replacement of SiO_2 is proposed. SiO_2 has ideal interface properties, large band gap, low trap density etc. The prolonged usability of the most popular dielectric in silicon microelectronics, nitride SiO_2 layers (SiON), were adopted first [20], with undebatable advantages in terms of increased dielectric constant and beneficial effects against boron penetration in p-MOSFETs. With the

advent of 45 nm technology, the first breakthrough innovation at the heart of the bulk MOSFET architecture, the introduction of high-k dielectrics has started to become a reality [21, 22]. It has become clear that significant innovations will be necessary to make the ultimate MOS a reality. Consistently, the technology boosters and new device concepts have been identified by the ITRS to flank the traditional dimension, doping, and voltage scaling. These new options could give significant advantages in terms of intrinsic device performance, thus allowing microelectronics to maintain progress according to the so-called Moore's law.

1.5 Tunnel FET

Unlike the conventional MOSFET, the transport mechanism in tunnel FETs (TFETs) is based on band-to-band tunneling at the source-channel carrier injection (tunneling currents for both the subthreshold region as well as the superthreshold region of operation). The gate length can be scaled down to the tunneling barrier width as small as 10 nm, or even less than this, because tunneling takes place over a very small region [21, 22].

TFETs can be scaled down to ultra-short-channel region without any significant change in device characteristics. The device parameters are independent of the channel length; therefore, statistical variation of the threshold voltage, OFF- and ON- currents, respectively, with channel-length variation are absent. TFETs show reliable operation at both low and high temperatures because of the weak temperature dependence. The current-voltage characteristics is not limited by the thermal factor, $^{kT}/_{q}$. This allows the thermal limit of the conventional MOSFET to be overcome, like bringing down the subthreshold swing below 60 mV/dec at room temperature [23, 24].

As conventional MOSFETs are scaled down to ultra-short-channel region, tunneling from heavily doped junctions results in large parasitic leakage currents. The on-current of TFET is determined by tunneling and therefore tunneling is no longer an unwanted parasitic effect. Furthermore, the current increases exponentially in both on- and off-regions of operation with respect to conventional device [24, 25]. Explanation of the working of TFETs is outlined in Chapter 2.

1.6 FinFET

The Fin Field-effect Transistor (FinFET) [26] is one of the competitors that can overcome the undesirable SCEs. It can replace the traditional MOSFET for low power applications [27]. Gate in a FinFET controls the channel from more than one side and provides outstanding performance against SCEs and very high on to off current ratio.

Fig. 1.8 shows the three-dimensional schematic of a FinFET. The main feature of the FinFET is that its conducting channel is wrapped by a thin silicon fin from which it gains its name. The thickness of the fin determines the effective channel of the device. It has a vertical fin between large source and drain. The gate is placed at right angle to the fin and wraps over the whole fin. As such, FinFET is a three-dimensional structure in general, where the gate controls the channel from all the three sides. It can be classified as a multi-gate MOSFET. As expected, it has improved SCEs than planar MOSFETS [26, 28].

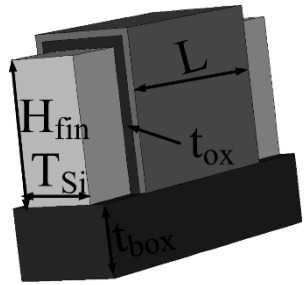

FIGURE 1.8 Three-dimensionalview of conventional FinFET

A special property of FinFET is fin width quantization, which says that the width can be increased by using multiple fins. The total transistor width of FinFET is expressed by [28]:

$$W = T_{Si} + 2H_{fin}$$

where T_{Si} and H_{fin} are the fin thickness and fin height, respectively. The total fin width for a FinFET having n parallel vertical fins is given b

$$W = n \times \left(T_{Si} + 2H_{fin} \right)$$

The working principle of a FinFET is similar to that of a MOSFET. The channel shows maximum conductance when there is no voltage on the gate terminal. As the voltage changes to positive or negative, the conductivity of the channel reduces. MOSFETs control the flow of voltage and current between the source and drain terminals. A high-quality capacitor is formed by the gate terminal. For n-MOSFETs, the semiconductor surface at the below oxide layer which is located between source and drain terminal is inverted from p-type to n-type by applying a positive gate voltage [28, 29].

When a small amount of voltage is applied to this structure, at positive gate to source voltage, a depletion region is formed. This depletion region is formed at the interface between Si and SiO_2. The positive voltage applied attracts electrons from the source terminal, and this forms the electron reach channel [29]. If we apply a voltage between the source and drain terminal, current will flow between source and drain terminals.

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2

DEVICE ARCHITECTURES: TFETS AND FINFETS

2.1 Introduction

This chapter presents a general survey on the different architectures of TFETs and FinFETs. TFETs and FinFETs have emerged as alternatives to MOSFETs due to their ability to withstand scaling. Scaled MOSFETs depict deteriorating performance with high leakage currents and poor subthreshold swings. While TFETs which operate on interband tunnelling can achieve theoretical subthreshold swings below 60 mV/dec, FinFETs, which are structural modifications of MOSFETs, can have reduced subthreshold swing as well, due to the greater influence of the gate on the fin structure. This chapter briefly explores some of the architectures of both devices in order to provide to readers an overview of the existing styles of geometry.

2.2 TFET Architectures

Geometry of Conventional TFETs

A conventional TFET geometry is shown in Fig. 2.1. The biasing conditions for *p*-type and *n*-type TFETs are tabulated in Table 1.1.

In an n-TFET, the application of positive gate voltage suppresses the energy bands at the *p+*-source- *i*-channel junction, causing the valence band of the source to line up with the conduction band of the channel. The tunnel barrier is approximated as a triangular barrier with reduced tunnel width [1]–[3]. The electrons from the valence band of the source tunnels through the barrier into the conduction band of the channel, and are finally collected by the *n+*-drain through a positive bias.

This mechanism of transport in TFETs allows them to possess SS lesser than the thermal limit of 60 mV/dec in MOSFETs. The tunnel barrier acts as a filter that prevents the passage of high and low energy Fermi tails, whereas

in MOSFETs thermionic emission allows the transmission of high-energy Fermi tails. TFETs also exhibit low off current due to their carrier transport mechanism [1]. SCEs are minimized owing to the dependence of the total current on the tunnel current concentrated at the tunnel junction. The advantage of TFETs is its compatibility with CMOS fabrication techniques.

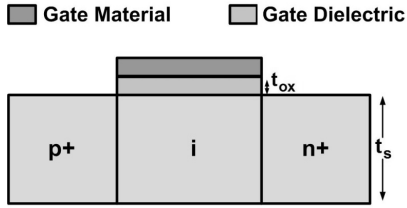

FIGURE 2.1 Geometry of a conventional TFET

TABLE 2.1 Modes of operation in TFETs, convention of source and drain regions and biasing conditions

Mode of Operation	Source	Drain	Bias
p-type	n+	p+	$V_{GD} < 0$; $V_{SD} < 0$
n-type	p+	n+	$V_{GS} > 0$; $V_{DS} > 0$

Evolution of TFETs

The idea of TFETs was first conceptualized by Stuetzer in 1952 before the invention of Esaki tunnel diodes, when he fabricated a *p-n* junction and explained its principle of operation under conditions of reverse bias [4]. He termed it "fieldistor". His paper discussed the effect of the position of the control electrode on the device characteristics, showing the presence of ambipolarity in the device. In 1977, Quinn *et al.* proposed the idea of a surface tunnel junction by substituting the degenerate n-type source of a MOSFET by a highly degenerate p-type source [5]. The paper mentioned the requirement of an abrupt junction and maximum band bending. The main focus of the work was subband splitting near to the tunnel junction, and the scope of determining the phenomenon experimentally. In 1987, Banerjee *et al.* presented a three-terminal device and reported the presence of Zener tunneling in the device [6]. The authors calculated the tunneling current by approximating the shape of the tunnel barrier as triangular. Takeda *et al.* proposed and characterized a band-to-band tunneling MOS device, and highlighted the negligible SCEs associated with

the 'Silicon quantum device' [7]. In 1992, Baba proposed the surface tunnel transistor (STT), an alternative version of Quinn's device, where he commented on the use of a gate to control negative differential resistance (NDR) in the forward bias state [8]. In 1995, Reddick and Amartunga proposed a gate controlled *p+-p-n+* structure of the STT, and produced experimental as well as simulation results to explain interband tunneling in STTs [9]. They also presented the basic formula for barrier height at the tunnel junction, which finds its use in analytical modeling of TFETs. In 1996, Uemura and Baba first demonstrated NDR in two planar-type STTs based on GaAs and InGaAs [10]. The gating of the vertical TFET was proposed by Hansch *et al.* in 2000 [11]. In 2004, the Silicon-on-insulator TFET was first proposed by Aydin *et al.* [12].

Modifications of Tunnel FETs

This section reports the next phase of development of TFETs after the establishment of fundamental *p-i-n* geometry. The significant architectures of TFETs proposed so far are presented here in brief, along with the types of analyses performed on those architectures. To maintain an organized discussion, a TFET architecture accompanied by modifications or associated improvements is presented in the following paragraphs.

Knoch and Appenzellar proposed the Tunneling Carbon Nanotube FETs in 2004, and discussed the methods to reduce the tunneling probability at the tunnel junction [13]. The one-dimensionality of carbon nanotube results in efficient band-to-band tunneling. A minimum SS of 15 mV/dec was achieved for low drain bias in the band-to-band tunneling regime.

Boucart and Ionescu proposed Double-Gate TFETs [14, 15] by introducing two gate terminals, one on the front and the other on the back, thus increasing the influence on the tunnel junction. The device was reported to offer a boosted on current as high as 0.23 mA, improved off current less than 1 fA and sub-60 mV/dec SS equal to 57 mV/dec. Toh *et al.* proposed a DG TFET with a silicon germanium source to modulate the tunnel barrier at the tunnel junction, thus resulting in enhanced on-current and sub-kT/q subthreshold swing [16]. DG TFETs using an InAs/Si heterojunction at the source-channel tunnel junction were reported by Ahish *et al.* to reduce the tunnel window and boost the on current [17].